UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,886	09/30/2003	Hyunjun Kim	P16828	9223

7590 12/30/2004

Buckley, Maschoff, Talwalkar & Allison LLC
Five Elm Street
New Canaan, CT 06840

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,886	KIM ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,084,779 (hereafter Fang)

Fang discloses, referring to figure 4b, an apparatus, comprising: a first voltage plane (20); a signal layer (22) on one side of the first voltage plane; a second voltage plane (14) on the other side of the first voltage plane and a floating trace (48) on the signal layer, wherein the floating trace is electrically connected to the second voltage plane [claim 1], wherein the first voltage plane is a power plane (20) and the second voltage plane is a ground plane (14) [claim 2], wherein the floating trace and the second voltage plane are electrically connected via a plated through hole (30) [claim 5], wherein the floating trace is a microstrip line (by definition, based on the "signal line over voltage plane structural arrangement) [claim 6], wherein the microstrip line provides impedance damping (see abstract) [claim 7], wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane (see abstract) [claim 8], wherein the first voltage plane, the signal layer, and the second voltage plane are separated by a dielectric material (24) [claim 9], wherein the apparatus is a printed circuit board [claim 10], wherein the printed circuit board is associated with at least one

of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model (col. 4, lines 5-20) [claim 11], further comprising: a second signal layer (16) [claim 12]: a second floating trace (40) on the second signal layer [claim 13].

Similarly, Fang discloses referring to figure 4b, an apparatus, comprising: a first voltage plane (14); a signal layer (12) on one side of the first voltage plane; a second voltage plane (20) on the other side of the first voltage plane and a floating trace (46) on the signal layer, wherein the floating trace is electrically connected to the second voltage plane [claim 1], wherein the first voltage plane is a ground plane (14) and the second voltage plane is a power plane (20) [claim 3],

Additionally, Fang discloses, a method, comprising: providing a first voltage plane (20); providing a signal layer (22) on one side of the first voltage plane; providing a second voltage plane (14) on the other side of the first voltage plane; and providing a floating trace (48) on the signal layer, wherein the floating trace is electrically connected to the second voltage plane [claim 14], further comprising: positioning the floating trace in the signal layer to reduce cross-talk with a neighboring signal line (see abstract) [claim 15], further comprising: providing a second signal layer (18); and providing a second floating trace (42) on the second signal layer [claim 16], wherein providing the floating trace comprising: providing a microstrip line on the signal layer [claim 17].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang in view of US 4,362,899 (hereafter Borrill).

Fang discloses the claimed invention as described above except Fang does not specifically disclose wherein the signal layer includes a plurality of floating traces, each floating trace being (i) electrically connected to the second voltage plane and (ii) not directly connected to other floating traces on the signal layer [claim 4]. Borrill teaches providing a plurality of floating shield tracks not directly connected to each other and

disposed alongside signal traces (see figure 1 and col. 1, lines 30-55). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to provide a plurality of the shield tracks taught by Borrill in the invention of Fang. The motivation for doing so would have been to provide local cross-talk suppression in the signal lines.

Similarly, Fang discloses a printed circuit board, comprising: a signal layer (22); a power plane (20) under the signal layer and separated from the signal layer by a dielectric material (24); a ground plane (14) under the power plane and separated from the power plane by the dielectric material, wherein a microstrip line (48) is (i) electrically connected to the ground plane via a plated through hole (30) passing through the dielectric material and the power plane.

Fang does not specifically disclose wherein the signal layer includes a plurality of loating traces, each floating trace being (i) electrically connected to the second voltage plane and (ii) not directly connected to other floating traces on the signal layer [claim 18]. Borrill teaches providing a plurality of floating shield tracks not directly connected to each other and disposed alongside signal traces (see figure 1 and col. 1, lines 30-55). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to provide a plurality of the shield tracks taught by Borrill in the invention of Fang. The motivation for doing so would have been to provide local cross-talk suppression in the signal lines. Additionally, the modified invention of Fang teaches wherein the microstrip lines provide impedance damping and reduce resonance between the power plane and the ground plane.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,243,261 (hereafter Janik) in view of Fang.

Janik discloses a PCB coupled to a DRAM [claim 19] and a processor [claim 20]. Janik does not disclose the particulars of the PCB. Fang teaches a printed circuit board, including; a first voltage plane (20), a signal layer (22) on one side of the first voltage plane, a second voltage plane (14) on the other side of the first voltage plane, and a floating trace (48) on the signal layer, wherein the floating trace is electrically connected to the second voltage plane. Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the PCB taught by Fang in the invention of Janik. The motivation for doing so would have been to use a circuit board with enhanced protection against cross talk, resulting in a more reliable device.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose shielded PCBs:

US 4,498,122 Rainal,

US 5,315,069 Gebara.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800